CLAIMS

What is claimed is:

1. A method for producing a liner mask on a semiconductor structure comprising:

providing an amorphous liner layer on a top side of the semiconductor structure in a deposition process at a first temperature;

annealing the amorphous liner layer at a second temperature, being higher than the first temperature, for increasing a degree of crystallisation and for generating at least a semi-crystalline liner layer whose etching rate in a predetermined etchant is higher than an etching rate of the amorphous liner layer;

performing an implantation of extrinsic ions in a subregion of the at least semi-crystalline liner layer for decreasing the etching rate of the subregion in the predetermined etchant and creating a etch selectivity between the subregion complementary subregion and the subregion in the predetermined etchant; and

selectively removing of the to the subregion complementary subregion opposite to the subregion in a etching step in the predetermined etchant for completing the liner mask.

2. The method of claim 1, where the semiconductor structure comprises a trench and that the implantation is performed so that the complementary subregion lies in the trench.

3. The method of claim 2, where the first temperature is between approximately 400°C and approximately 600°C and the second temperature is between approximately 700°C and 1100°C.

4. The method of claim 1, where on the top side of the semiconductor structure underneath the liner layer, a further liner layer is provided, on which the etching step for selectively removing of the complementary subregion stops.

5. The method of claim 4, where the first temperature is between approximately 400°C and approximately 600°C and the second temperature is between approximately 700°C and 1100°C.

6. The method of claim 1, where the first temperature is between approximately 400°C and approximately 600°C and the second temperature is between approximately 700°C and 1100°C.

7 The method of claim 6, where the semiconductor structure comprises a trench and that the implantation is performed so that the complementary subregion lies in the trench.

8. The method of claim 1, wherein the liner layer includes silicon and the extrinsic ions include boric ions or boron ions.

9. The method of claim 8, where the semiconductor structure comprises a trench and that the implantation is performed so that the complementary subregion lies in the trench.

10. The method of claim 9, where on the top side of the semiconductor structure underneath the liner layer, a further liner layer is provided, on which the etching step for selectively removing of the complementary subregion stops.

11. The method of claim 10, where the first temperature is between approximately 400°C and approximately 600°C and the second temperature is between approximately 700°C and 1100°C.

12. A liner mask for a trench capacitor comprising an isolation collar in a substrate being single-sided electrically connected with the substrate by a buried contact, for a semiconductor memory cell with a planar selection transistor provided in the substrate and connected over the buried contact, where the liner mask defines a single-sided contact region and an other-sided isolation region of the buried contact in a trench for the trench capacitor.

13. The liner mask of claim 12, where the trench for the trench capacitor comprises a conductive filling with a region filling the trench above the isolation collar and from which a subregion is removed using the liner mask and which is filled with an isolating filling in the following for completing the isolating region.

14. The liner mask of claim 13 where the subregion is transformed into an oxidized subregion after the selective etching by means of an oxidation.